

Appl. No. 10/707,968
Amdt dated November 21, 2006
Response to Office Action of August 21, 2006

REMARKS/ARGUMENTS

Claim Objections

Claims 29 and 37 have been objected to by the Examiner for various informalities. Applicants in response have amended these claims, correcting the various informalities as indicated by the Examiner. Applicants therefore submit that the objections to the claims have been traversed and respectfully request their withdrawal.

Rejection under 35 USC § 102(b)

Claims 1-5, 8, 10-12, 15, 16, 18-20, 22, 23, 25, 26-28, 30-36, 38-40 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,397,909 ("Moslehi"). Applicants respectfully disagree.

Claim 1 recites a method of fabricating a gate electrode by providing a gate stack which includes a gate dielectric on a substrate and a gate layer over the gate dielectric. A metal layer is provided over the gate layer and a reaction consumes substantially all of the gate and metal layers to form a resulting layer which serves as the gate electrode. The gate electrode layer is in contact with the gate dielectric layer. Claim 16 recites a method for forming an integrated circuit which includes providing a substrate prepared with a gate stack. Like claim 1, the gate layer of the gate stack is reacted with a metal layer to substantially consume all the material of the layers to form a resulting layer which serves as the gate electrode which contacts the gate dielectric. Claim 10 recites a gate electrode which comprises a first material and a metal which have been substantially consumed during a reaction with one another. Like claim 1 or 16, the gate electrode is in contact with the gate dielectric.

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Moslehi, in contrast, describes elevated source/drain transistors. The transistor includes a multilayered gate stack disposed over a gate dielectric layer. The gate stack includes a reacted refractory metal contact on top of the gate stack (element 74 or 100). It appears that the Examiner, in rejecting the claims, has equated the contact layer of Moslehi with the gate electrode of the present claims. However, even assuming that the contact layer can be equated to the gate electrode, this still fails to anticipate the invention as claimed. In particular, the contact layer of Moslehi is separated from the gate dielectric by lower and upper gate regions. See e.g., Moslehi, Fig. 9 or 19 (elements 50, 68 and 72 or 50, 88 and 100). Moslehi nowhere teaches or suggests providing a contact layer which is in contact with the gate dielectric. Applicant therefore submits that claims 1, 10 and 16 and their dependent claims 2-9, 11-15 and 17-40 are patentable over Moslehi.

Claim 41 stands rejected under 35 U.S.C. 102(b) as being anticipated by US 5,952,701 (Bulucea et al.). Applicants respectfully disagree.

Claim 41 recites an integrated circuit with a transistor disposed on a substrate. The transistor comprises a gate stack which a gate dielectric on the substrate and a gate electrode disposed on and in contact with the gate dielectric. The gate electrode is formed from an amorphous or polycrystalline first layer and a metal layer which have been substantially consumed during reaction with one another caused by annealing, wherein problems associated with inversion and agglomeration associated with formation of the transistor is reduced.

Bulucea et al., on the other hand, describes channel-junction insulated gate field-effect transistors. Like Moslehi, the silicidic contact layer is separated from the gate dielectric by the polysilicon gate. Providing a gate stack having a gate electrode in contact with the gate dielectric layer, wherein the gate electrode is formed from an amorphous or polycrystalline first layer and a metal layer which been substantially consumed during reaction with one another

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caused by annealing, as required by claim 41, is nowhere taught or suggested by Bulucea et al. Applicants therefore submit that the rejection based on Bulucea et al. has been traversed and respectfully request its withdrawal.

Rejection under 35 USC § 103(a)

Claims 9, 13, 17, 21, 24 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi, US5,397,909 in view of US 5,705,417 ("Tseng"). Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moslehi in view of US 6,084,279 ("Nguyen et al."). Applicants respectfully disagree.

As discussed above, Moslehi fails to teach or suggest providing a gate electrode in direct contact with a gate dielectric, wherein the gate electrode is formed from a gate layer and a metal layer which have been substantially consumed by a reaction. Combining Tseng and/or Nguyen et al., as suggested by the Examiner, fails to cure the defect of Moslehi. As for Tseng, it discloses a gate having sequential gate dielectric, polysilicon and silicide layers. See Tseng, Fig. 6G (elements 62, 64 and 78). Nguyen et al. describes gate stack having a sequential layers of gate dielectric, silicon nitride, silicon and silicide layers. See Nguyen et al., Fig. 8 (elements 20, 66, 68 and 85). As such, the silicide layer in Tseng or Nguyen et al. is separated from the gate dielectric by at least one intermediate layer, not in direct contact with the gate dielectric as required by the present claims. Therefore, Applicants submit that Moslehi, Tseng and Nguyen et al., alone or in combination, fail to teach or suggest the invention as claimed.

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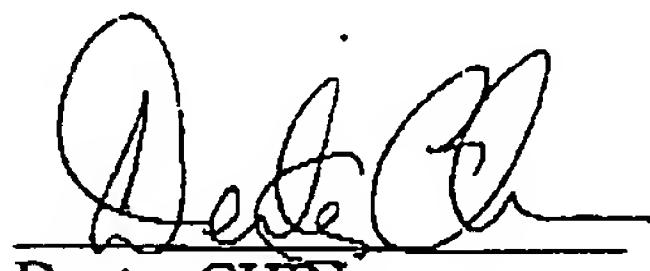
Conclusion

In view of the foregoing, Applicants believe that all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Should the Examiner believe that a telephone conference would expedite prosecution of this Application, please telephone the undersigned attorney at his number set out below.

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Respectfully submitted,



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